1. (AMENDED) An apparatus comprising:

one or more logic circuits configured to provide logical operation, wherein said one or more logic circuits comprise (i) programmable logic elements and (ii) non-programmable logic elements within a programmable logic device (PLD).

2. The apparatus according to claim 1, wherein said one or more logic circuits comprise variable width logic circuits.

3. The apparatus according to claim 2, wherein a width of each of said one or more logic circuits is determined in response to one or more input signals.

4. The apparatus according to claim 1, wherein each of said one or more logic circuits is configured to receive a first one or more inputs, wherein said first one or more inputs comprise multi-bit or single-bit signals in a serial or a parallel configuration.

5. The apparatus according to claim 1, wherein each of said one or more logic circuits comprises a hard wired multiplier.

6. The apparatus according to claim 1, wherein said one or more logic circuits are configured to perform a cyclic redundancy check (CRC) functions.

7. The apparatus according to claim 1, wherein each of said one or more logic circuits is configured to present an output.

Cont A1

8. (AMENDED) The apparatus according to claim 7, wherein each of said one or more outputs comprise intermediate signals.

Sub C1

9. The apparatus according to claim 7, further comprising:

an adder circuit configured to receive said one or more outputs.

Sub B3

10. (AMENDED) The apparatus according to claim 9, further comprising a routable interconnect circuit configured to route signals to/from one or more of said non-programmable elements.

11. (AMENDED) The apparatus according to claim 10, further comprising a number of registers configured to increase a throughput of said one or more logic circuits.

12. The apparatus according to claim 1, wherein each of said one or more logic circuits comprise an input portion configured to store one or more input signals.

13. The apparatus according to claim 12, wherein each of said one or more logic circuits comprises an output portion configured to store an output.

15. (AMENDED) An apparatus comprising:

means for receiving one or more input signals; and

means for performing logical operation on said input signals using (i) programmable logic elements and (ii) non-programmable logic elements within a programmable logic device (PLD).

16. (AMENDED) A method for computing in a programmable logic device (PLD) comprising the steps of:

(A) receiving one or more input signals;

(B) performing logical operation on said one or more input signals with (i) programmable logic elements and (ii) non-programmable logic elements within said programmable logic device.

17. (AMENDED) The method according to claim 16, further comprising the step of:

(C) generating one or more intermediate signals.

18. The method according to claim 17, wherein step (C) further comprises:

multiplying said one or more input signals.

19. The method according to claim 16, wherein step (B) further comprises:

receiving said one or more outputs and adding said one or more outputs.

20. The method according to claim 16, wherein step (B) further comprises:

routing said one or more outputs.

Please add the following new claim.

21. (NEW) The apparatus according to claim 1, wherein said non-programmable elements comprise dedicated logic having a specific functionality.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (AMENDED) An apparatus comprising:

one or more logic circuits configured to provide logical operation [computation], wherein said one or more logic circuits comprise (i) programmable logic elements and (ii) non-programmable logic elements [dedicated logic] within a programmable logic device (PLD).

8. (AMENDED) The apparatus according to claim 7, wherein each of said one or more outputs comprise [partial product] intermediate signals.

10. (AMENDED) The apparatus according to claim 9, further comprising a routable interconnect circuit configured to route signals to/from one or more of said non-programmable elements.

11. (AMENDED) The apparatus according to claim 10 [11], further comprising a number of registers configured to increase a throughput of said one or more logic circuits.

15. (AMENDED) An apparatus comprising:

means for receiving one or more input signals; and

means for performing logical operation on said input signals using (i) programmable [computing comprising dedicated] logic elements and (ii) non-programmable logic elements within a programmable logic device (PLD).

16. (AMENDED) A method for computing in a [Programmable Logic Device] programmable logic device (PLD) comprising the steps of:

(A) receiving one or more input signals;

(B) performing logical operation on said one or more input signals [computing] with [dedicated] (i) programmable logic elements and (ii) non-programmable logic elements within said programmable logic device [(PLD)].

17. (AMENDED) The method according to claim 16, further comprising the step of:

(C) generating one or more intermediate [partial product] signals.

21. (NEW) The apparatus according to claim 1, wherein said non-programmable elements comprise dedicated logic having a specific functionality.